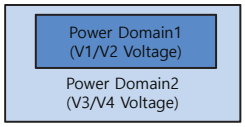
Need for Inter Power Domain (IPD) flow

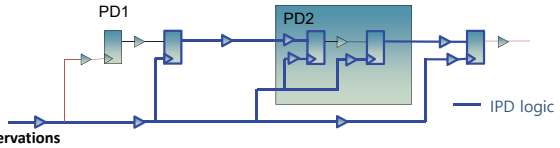
- **IPD timing signoff has become a critical part of today's timing closure flow**
- **Challenges with IPD timing signoff**
  - **High number of IPD analysis corners**
    - Difficult to exhaustively analyze all voltage combinations
  - **High cycle time and compute required for IPD signoff**
  - **Comprehend different constraints for each IPD corner operating at various voltage and frequency (DVFS) conditions**
  - **Accurate analysis needed at each IPD corner: traditional derates based approach can be highly inaccurate**
- **An efficient sign-off / ECO solution to address above challenges is must for quicker time-to-market**

# Power Domains	# Operating Voltages	# Voltage Corners
2	2	4
3	3	27
4	4	256
5	5	3125



Power Domain1 Voltage	Power Domain1 Clock Frequency	Power Domain2 Voltage	Power Domain2 Clock Frequency
V1	A MHz	V3	C MHz
V1	A MHz	V4	D MHz
V2	B MHz	V3	C MHz
V2	B MHz	V4	D MHz

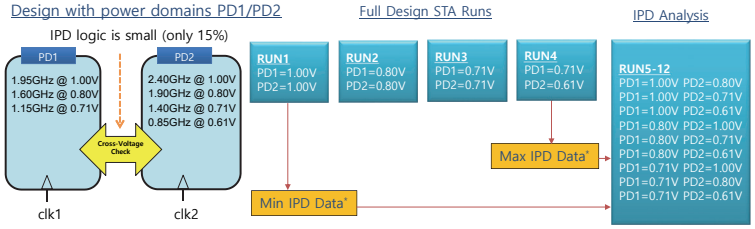
IPD logic analysis



- **Observations**
  - **IPD logic is small (< 20% on average). Full analysis runs for voltage crossing paths is costly and not necessary**
  - **Significant number of timing signoff runs related to IPD analysis**
- **Solution**
  - **IPD-logic only analysis results in significant runtime/memory gains**
    - Only highlighted IPD logic in below picture analyzed, non-IPD logic is not analyzed
  - **Above facilitates combining 10+ IPD corners can be combined into a single run using Tempus Concurrent Multi-Mode Multi-Corner (CMMMC)* solution**
    - CMMMC analysis supports separate DVFS constraints (clock definitions, uncertainty, derates etc) for each corner
  - **Arrival windows/slews for non-IPD aggressors are obtained from traditional bounding corner runs**
    - Min/Max IPD aggressor data written from bounding full analysis runs and read during IPD analysis
  - **Seamless integration with Tempus-ECO**

** CMMMC is covered in the last slide*

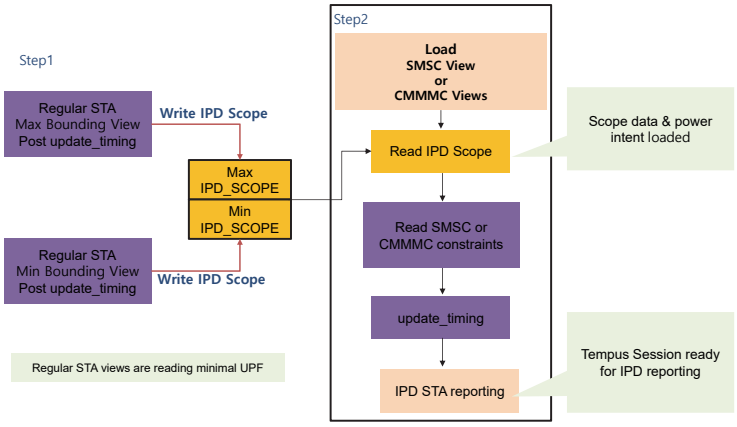
Tempus based Efficient Inter Power Domain Analysis



- **Runs 1-12 form the exhaustive voltage combinations required for timing signoff**
  - **Runs 1-4 cover the traditional signoff corners and Runs 5-12 cover the IPD corners**
- **Full design analysis runs generates the min (Run1) and the max (Run4) IPD aggressor data**
  - **IPD data contains slew, waveform, arrival windows etc. on non-IPD aggressors**
- **Min/Max IPD data are read during IPD analysis to get the bounding aggressor slews and windows**

** In this design, arrival windows for 99.7% pins across all IPD corners are bounded by conventional min/max STA corners*

Overall flow



Results: Conventional STA vs IPD analysis

- **Runtime and Memory usage**
  - ***Achieved 12.5X runtime gain and 81.4% memory reduction***

IPD Analysis (12 view) (till UT -full)		Conventional STA (till UT -full)				Improvement	
Runtime (min)	Peak Memory (GB)	1 views STA time (min)	12 views STA time (min)	1 Views STA memory (GB)	12 Views STA memory (GB)	Runtime	Memory
11	25	11.5	12 * 11.5 = 138	11.2	12 * 11.2 = 134.4	12.5X	81.4%

- **Correlation**
  - **# of IPD path : 2684**

RC corner	Temperature/RC corner : 125C/RCmax							
With SI With Derates	RUN5	RUN6	RUN7	RUN8	RUN9	RUN10	RUN11	RUN12
Within 3% error	99.96%	99.73%	99.03%	99.62%	99.59%	99.07%	99.63%	99.63%
Within 5% error	100.00%	100.00%	100.00%	100.00%	99.93%	100.00%	100.00%	100.00%
Paths within 10 ps	1816	2518	1956	2438	2616	2088	2527	2639

Summary

- **With design sizes increasing and the number of power domains, specialized solution for inter-power domain analysis and closure is critical**
- **Benefits from proposed solution**

Metrics	Benefits
Reduced design TAT	Significant runtime/memory improvements 10+ IPD corners with CMMMC at the cost of single full design analysis Integrated ECO solution
Improved quality of silicon	Exhaustive analysis of IPD voltage corners
Decreased complexity	IPD focused analysis and reporting Reduced number of runs with CMMMC

- **Future works**
  - **Tempus ECO evaluation**
  - **New IPD reporting infrastructure validation**